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09/557,164	04/25/2000	William J. Dally	2789.2004-001	9280

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EXAMINER	
BAYARD, EMMANUEL	
ART UNIT	**PAPER NUMBER**
2631	

DATE MAILED: 06/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/557,164	DALLY ET AL.	
	Examiner	Art Unit	
	Emmanuel Bayard	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-66* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-66* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is in response to RCE filed on 3/28/05 in which claims 1-68 are pending.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 19-32, 44-49, 51-54, 59-64 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claims 19, 27, 51, 59-60, 63 recite the limitation "the delay elements" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

4. Claim 23 recites the limitation "the parallel delay elements" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

5. Claim 44 and 48 recite the limitation "the delay elements" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claims 20-22, 24-26, 28-32 45-49, 52-54, 61-64 are likewise rejected because they depend on base rejected claim.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-17, 23-26, 39-42, 55-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over O'Sullivan et al U.S. Patent No 6,259,755 B1 in view of Drost et al U.S. Patent 6,028,903.

As per claim 1, a data input (see figs. 6-12, 15-18 element Fdata 61); plurality delay means for applying different delays to the data input to provide plural delayed data signals (see fig.15); a phase comparator or a phase detector is the same as the claimed (data output means for combining) (see figs 6-12, 15-19 element PFD and col.6, lines 5-30 and col.7, lines 55-67 the delayed data signals into a data output having a rise or fall transition time determined by different delays applied to the data inputs wherein the rise or fall transition time of the data output signal is greater than the rise or fall transition time of the data input (see figs. 6-12 element 63,, 102, 1102, 1103 and col.7, lines 2-10 and col.8, lines 23-50).

However O'Sullivan et al does not teach plurality delay means that apply different delays to the data input **in parallel** to provide plural delayed data signals.

Drost et al teaches plurality delay means that apply different delays to the data input **in parallel** to provide plural delayed data signals (see abstract and fig.1 elements line1, line2 and col.5, lines 10-67).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Drost into O'Sullivan as to determine the occurrence at every possible transition instant of the incoming data as taught by Drost (see abstract).

As per claims 2, Drost does include parallel delay connection (see abstract and fig.1 elements line1, line2 and col.5, lines 10-67). Furthermore implementing such teaching into O'Sullivan would have been obvious to one skilled in the as to determine the occurrence at every possible transition instant of the incoming data as taught by Drost (see abstract).

As per claim 3, the data transmitter O'Sullivan et al teaches a clock signal applied the delay elements and different delays are applied to the data input (see fig.8).

As per claims 4, 8, 24, 40, 56 O'Sullivan and Drost in combination would teach a plural driver circuits as to accurately determine the occurrence at every possible transition instant of the incoming data.

As per claims 5, 9, 25, 41, 57, O'Sullivan and Drost in combination would teach CMOS inverters as to accurately determine the occurrence at every possible transition instant of the incoming data.

As per claims 6, 10, 26, 42, 58 O'Sullivan and Drost in combination would teach a load capacitance as to accurately determine the occurrence at every possible transition instant of the incoming data.

As per claims 7, 23, 39, 55 are rejected under the same rational as describe in claim 1 above.

As per claim 11, O'Sullivan and Drost in combination would teach includes data output is proportional to bit time as to accurately determine the occurrence at every possible transition instant of the incoming data.

As per claims 12, 15 the circuit of O'Sullivan does include a supply voltage (see fig.8) to control the delay elements.

As per claim 13-14, 16-17 O'Sullivan et al discloses a circuit to control power supply voltage to the delay elements (see fig.8 element 67), the circuit comprising: a first and second delay elements (see fig.15), each receiving a common clock signal and a phase comparator (see fig.15 elements PFD) which compares the outputs of the first and second delay elements and control a supply voltage applied to the first and second delay elements to control phase difference of the outputs (see col.11, lines 19-25).

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 18-22, 27-33, 43-54, 59-66 are rejected under 35 U.S.C. 102(b) as being anticipated by O'Sullivan et al U.S. Patent No 6,259,755 B1.

As per claims 18, 50 and 66, O'Sullivan et al teaches a data transmitter comprising: a data input (see figs. 6-12, 15-18 element Fdata 61); a bit clock (see figs 6-12 element Fclk and col.6, lines 20-30) a rise or fall transition time control (see figs. 6-12 element 63,, 102, 1102, 1103 and col.7, lines 2-10 and col.8, lines 23-50) for

receiving the data input and providing a controlled data signal, the transition time control controlling the transition time of the controlled signal to be proportional to bit time of the bit clock (see col.6, lines 52-67) .

As per claims 19, 27, 30 and 51, the data transmitter of O'Sullivan et al teaches a clock signal applied the delay elements and different delays are applied to the data input (see fig.8 element 67).

As per claim 43, the data transmitter of O'Sullivan et al inherently includes data output is proportional to bit time.

As per claims 44, 47, 59, 62 the circuit of O'Sullivan et al does include a supply voltage (see fig.8 element 67) to control the delay elements.

As per claims 28-29, 31-32, 45, 48, 60, 63 O'Sullivan et al discloses a circuit to control power supply voltage to the delay elements (see fig.8 element 67), the circuit comprising: a first and second delay elements (see fig.15), each receiving a common clock signal and a phase comparator (see fig.15 elements PFD) which compares the outputs of the first and second delay elements and control a supply voltage applied to the first and second delay elements to control phase difference of the outputs (see col.11, lines 19-25).

As per claims 46, 49, 61, 64 the transmitter of O'Sullivan et al does include a first and second delay elements having a sequence of n elements and a clock signal frequency (see fig.15).

As per claims 20, 52, the data transmitter of O'Sullivan et al includes a plural driver circuits (see col.7, lines 48-50).

As per claims 21, 53 the data transmitter of O'Sullivan et al inherently includes CMOS inverters.

As per claims 22, 54 the data transmitter of O'Sullivan et al inherently includes load capacitance.

As per claim 65 O'Sullivan et al includes a data transmitter comprising: a data input (see figs. 6-12, 15-18 element Fdata 61); plurality delay means for applying different delays to the data input to provide plural delayed data signals (see fig.15); a phase comparator or a phase detector is the same as the claimed (data output means for combining) (see figs 6-12, 15-19 element PFD and col.6, lines 5-30 and col.7, lines 55-67 the delayed data signals into a data output having a rise or fall transition time determined by different delays applied to the data inputs wherein the rise or fall transition time of the data output signal is greater than the rise or fall transition time of the data input (see figs. 6-12 element 63,, 102, 1102, 1103 and col.7, lines 2-10 and col.8, lines 23-50).

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Thacker U.S. patent No 5,313,501 teaches a method and apparatus for deskewing.

Dortu U.S. Patent No 6,043,694 teaches a lock arrangement.

Yashikawa U.S. Patent No 6,157,229 teaches a skew compensation device.

Banwell et al U.S. patent No 6,285,722 B1 teaches a method and apparatus for variable bit rate.

Tucci U.S. Patent No 5,097,489 teaches a method for incorporating window strobe.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is 571 272 3016. The examiner can normally be reached on Monday-Friday (7:Am-4:30PM) Alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 571 272 3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Emmanuel Bayard
Primary Examiner
Art Unit 2631

6/9/05

EMMANUEL BAYARD
PRIMARY EXAMINER